

**Fabrication of long wavelength array
by in-situ molecular beam epitaxy
Monthly report No. 5
(contract No. DAAB07-91-C-K762)**

During this program period, we have designed a readout circuit based on cryo CMOS technology with device features of 1.0 micron dimensions. The input circuit as depicted in Fig. 1 uses a direct injection approach and the cell is 2 mil x 2 mil dimension. The concept of direct injection readout is also applied for the InSb/InAsSb pin detector, since the reverse bias impedance of pin is reasonably high.

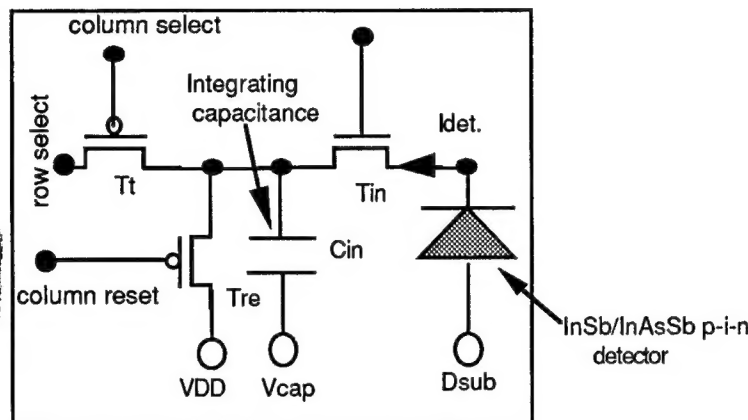


Fig. 1 CMOS Readout unit cell compatible with InSb/InAsSb pin detector

In Fig. 1, T_{in} at the input is a p-channel MOSFET (since our detector injects holes due to IR radiation) and the voltage at the gate is used to set the reverse bias for the InSb/InAsSb pin detector. C_{in} is the integrating capacitor where the charge converted from the incident IR radiation is stored. Since we use 1.0 micron devices for the active devices, the real estate available is reasonably large for the capacitor along with a thin gate oxide on the order of 160-200 Å. T_t is the cell-access PMOSFET which is used to select the rows and columns by applying appropriate pulses on the row and column buses. T_{re} is another reset PMOSFET which is used to reset the pixel. The various clock signals are generated by dynamic CMOS shift registers which are configured at the periphery of the cell matrix. At the end of an integration time, the cell is accessed, the signals read out through a source follower at the output located at the end of the column bus and then the capacitor is reset. The access and reset FETs in each unit cell is stopped by CMOS clocks generated by the peripheral shift registers. As the clock signal propagates down the row register, the cells are sequentially accessed in each row, the signal is read by column by column basis and the storage capacitors in each row reset. Since we use CMOS registers, the power dissipation will be minimal with limited integration noise level. The integration time is adjustable from 0.4 to 99% of the frame time which is controlled by a frame pulse.

We have illustrated, in Fig. 2, the layout schematic for a unit pixel input circuit discussed above. We have done the basic cell design on 1.0 micron design algorithm and the design can be scaled up or down depending on the requirement. Our base-line approach would be a 50 micron x 50 micron pixel size compatible with 256x256 array size. The pixel could be scaled down to 1 mil x 1 mil size for arrays as large as 640x484 resolution. Since the CMOS process is highly advanced using state-of-the-art drain engineering technologies involving LDDs (lightly doped drain) using oxide sidewall spacers, hot-carrier effects are minimized to improve the reliability and performance of the circuits.

Fig. 2 Layout scheme for input circuit for MUX.

Several InSb/InAsSb strained superlattice (SSL) films have been grown in this period to test the spectral tunability over $10\mu\text{m}$. A cutoff edge at about $10.2\mu\text{m}$ is shown in Fig. 3, measured from the grown InSb/InAs_{0.13}Sb_{0.87} (200Å/200Å) SSL.

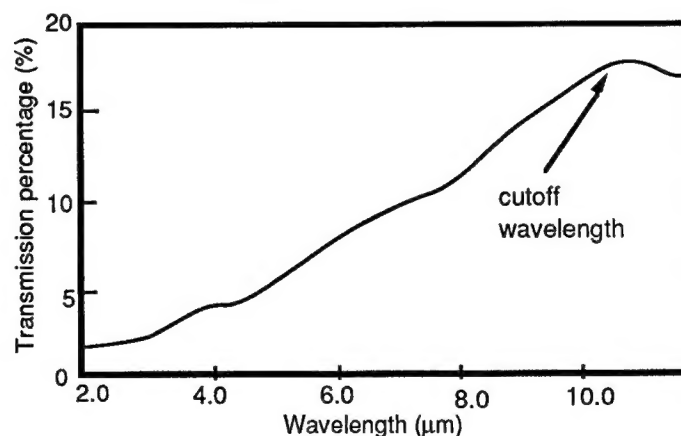


Fig. 3 Cutoff wavelength of InSb/InAs_{0.13}Sb_{0.87} SSL film measured by FTIR.

In summary, we have designed the readout circuit for InSb/InAsSb pin detector. The InSb/InAsSb SSL with a cutoff wavelength of $10.2\mu\text{m}$ has been successfully grown in our laboratory. The tasks set for this period were completed as planned.